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L3	9	(tick near4 counter).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:20
L4	41	(tick near4 counter).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:59
L5	18	(tick near4 counter).clm. and synchroniz\$5	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2006/10/25 15:59
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1 Minimal multitasking operating systems for real-time controllers

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Geoffrey H. Kuenning

October 1981 Proceedings of the 1981 ACM SIGSMALL symposium on Small systems and SIGMOD workshop on Small database systems

Publisher: ACM Press

Full text available: pdf(643.54 KB) Additional Information: full citation, abstract, references, index terms

In many dedicated microprocessor applications, a full-feature operating system is not required. A methodology is presented for the design of extremely minimal operating systems for such applications. The emphasis is on providing the most basic facilities quickly, without precluding later improvements and additions.

Virtual Hardware Prototyping through Timed Hardware-Software Co-Simulation Franco Fummi, Mirko Loghi, Stefano Martini, Marco Monguzzi, Giovanni Perbellini, Massimo Poncino



March 2005 Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05

Publisher: IEEE Computer Society

Full text available: pdf(208.94 KB) Additional Information: full citation, abstract, index terms

Designers of factory automation applications increasingly demand for tools for rapid prototyping of hardware extensions to existing systems and verification of resulting behaviors through hardware and software co-simulation. This work presents a framework for the timing-accurate co-simulation of HDL models and their verification against hardware and software running on an actual embedded device of which only a minimal knowledge of the current design is required. Experiments on real-life applicat ...

3 MINI-EXEC: a portable executive for 8-bit microcomputers



Thomas L. Wicklund

November 1982 Communications of the ACM, Volume 25 Issue 11

Publisher: ACM Press

Full text available: pdf(578.22 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: microprocessor control systems, multitasking, real-time executives, software portability

4 Let caches decay: reducing leakage energy via exploitation of cache generational



behavior

Zhigang Hu, Stefanos Kaxiras, Margaret Martonosi

May 2002 ACM Transactions on Computer Systems (TOCS), Volume 20 Issue 2

Publisher: ACM Press

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Additional Information: full citation, abstract, references, citings, index

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galsC: A Language for Event-Driven Embedded Systems

Elaine Cheong, Jie Liu

March 2005 Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05

Publisher: IEEE Computer Society

Full text available: pdf(178.34 KB) Additional Information: full citation, abstract, index terms

We introduce galsC, a language designed for programming event-driven embedded systems such as sensor networks, galsC implements the TinyGALS programming model. At the local level, software components are linked via synchronous method calls to form actors. At the global level, actors communicate with each other asynchronously via message passing, which separates the flow of control between actors. A complementary model called TinyGUYS is a guarded yet synchronous model designed to allow threadsa ...

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6 Formal languages: Towards direct execution of esterel programs on reactive



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Partha S. Roop, Zoran Salcic, M.W. Sajeewa Dayaratne

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Esterel is a system-level language for the modelling, verification and synthesis of control dominated (reactive) embedded systems. Existing Esterel compilers generate intermediate C code that is subsequently mapped to a suitable target processor. The generated code emulates the reactive features of the language due to lack of support for these features on traditional processors. The resultant code is thus inefficient and bulky. Therefore, Esterel is not so effective for resource constrained embe ...

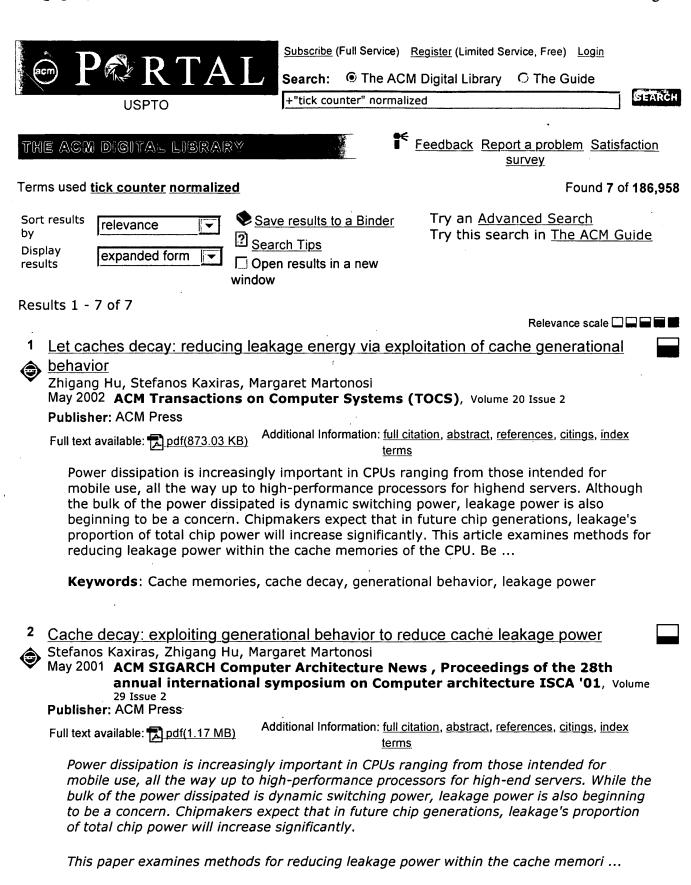
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8	Workshop on architectural support for security and anti-virus (WASSA): Towards the issues in architectural support for protection of software execution Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, Mrinmoy Ghosh March 2005 ACM SIGARCH Computer Architecture News, Volume 33 Issue 1 Publisher: ACM Press	
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10 ②	Cache decay: exploiting generational behavior to reduce cache leakage power Stefanos Kaxiras, Zhigang Hu, Margaret Martonosi May 2001 ACM SIGARCH Computer Architecture News, Proceedings of the 28th	

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٠	We present the first profiler for a compiled, non-strict, higher-order, purely functional language capable of measuring time as well as space usage. Our profiler is implemented in a production-quality optimising compiler for Haskell, has low overheads, and can successfully profile large applications. A unique feature of our approach is that we give a formal specification of the attribution of execution costs to cost centres. This specification ena	

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A Mechanism for Online Diagnosis of Hard Faults in Microprocessors

Fred A. Bower, Daniel J. Sorin, Sule Ozev

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7 Workshop on architectural support for security and anti-virus (WASSA): Towards the

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Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, Mrinmoy Ghosh

March 2005 ACM SIGARCH Computer Architecture News, Volume 33 Issue 1

Publisher: ACM Press

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